Undergrad Projects in the SLICE Lab (in Hardware Verification)

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Skills: Scala, functional programming, C++, RTL design / Verilog, frontend webdev, SMT, compilers, fuzzing

Projects:

- A High-Performance FFI Bridge between C++ and JVM for RTL Testbenches
- A Functional, High-Performance Testbench API
- High-Level Synthesis (HLS) of Verification IPs (VIPs) for FPGA Accelerated Simulation
- Functional, Introspectable Constrained Random API for Stimulus Embedding
- Coverage Specification API for Chisel
- Integration of Coverage Passes, Coverage Merging and Report Generation into chiseltest
- Mutation Testing for Chisel Circuits
- Waveform Visualization for Debug
- Fuzzing Hardware Models as a Proxy for Fuzzing Hardware

Detailed descriptions:
https://vighneshiyer.com/misc/ugrad-projects